

VIRTUAL MACHINE EMULATION IN THE MEMORY SPACE OF A PROGRAMMABLE PROCESSOR

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Abstract of the Disclosure

Apparatus and method for emulating a virtual machine within the physical memory space of a programmable processor using virtual functions having a format independent of the hardware architecture of the processor. The virtual functions are executed using an execution engine emulated in the processor. A symbol table maps the virtual functions to native functions in the memory space, and a gate call interface block accesses the symbol table and initiates execution of the corresponding native function in response to each executed virtual function. Execution of the corresponding native function operates to evaluate the concurrent execution of at least one other native function. In this way for example, standardized platform virtual code can be generated for a number of different types of processors and used to evaluate the native operational routines of each processor.